

	Ministry of Higher Education and Scientific Research - Iraq University of Baghdad College of Engineering Department of Computer Engineering	
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MODULE DESCRIPTOR FORM

نموذج وصف المادة الدراسية

Module Information					
معلومات المادة الدراسية					
Module Title	DIGITAL CIRCUIT DESIGN			Module Delivery	
Module Type	CORE			☒ Theory ☐ Lecture ☒ Lab ☐ Tutorial ☐ Practical ☐ Seminar	
Module Code	COE 203				
ECTS Credits	7				
SWL (hr/sem)	175				
Module Level	2		Semester of Delivery	3	
Administering Department	Computer Engineering		College	College of Engineering	
Module Leader	Ahmed Ubaid Salman		e-mail	ahmad.obaid@alnaji-uni.edu.iq	
Module Leader's Acad. Title	Asst. Prof		Module Leader's Qualification	PhD	
Module Tutor			e-mail		
Peer Reviewer Name			e-mail		
Review Committee Approval	24/08/2024		Version Number	1.1	

Relation With Other Modules			
العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	COE107		Semester 2
Co-requisites module	None		Semester

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	This program Specification provides a concise summary of the main features of the program of digital circuit design (DCD) and the learning outcomes that a typical student might reasonably be expected to achieve and demonstrate if he/she takes full advantage of the learning opportunities that are provided. It should be cross-referenced with the programmed specification.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1- Simplify & solved any Boolean equation until to 6 variables using K-map method. 2- Acknowledge how to design digital problem using finite state machine approach. 3- Analysis any sequential circuit of a digital system using Mealy and Moore state machine design. 4- Design practical & complex problem using multiple inputs and/or outputs. 5- Realize digital circuit design using various types of flip flops (FFs). 6- Separate between synchronous & asynchronous state machine approach in a design. Discuss all the problems of asynchronous design. 7- Design a digital circuit & solve practical problems by applying VHDL language in a design
Indicative Contents المحتويات الإرشادية	
Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	- Lectures. - Homework, Quizzes and Assignments. - Extracurricular Activities. - Tests and Exams. - In-class questions and Discussions. Student engagement during Lectures. - Individual / Group Projects - In- and Out-Class conversations.

Student Workload (SWL)

الحمل الدراسي للطالب

Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	79	Structured SWL (h/w) الحمل الدراسي المنتظم للطالب أسبوعياً	5
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	71	Unstructured SWL (h/w) الحمل الدراسي غير المنتظم للطالب أسبوعياً	5
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation

تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	3	10% (10)	3, 7, 11	LO #1-4
	Assignments	2	5% (5)	3, 9	LO # 1,2,3
	Lab.	6	20% (20)	1 -15	LO # 1-6
Summative assessment	Project	1	5% (5)	12	LO #1-4
	Mid Exam	1	10% (10)	15	LO # 3,4,5
	Final Exam	3 hr	50% (50)	16	LO # 1-6
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)

المنهاج الأسبوعي النظري

	Material Covered
Week 1	Introduction to synchronous sequential circuits with design methodology: State diagram, state table, reduction, binary assignment table and circuit realization. Then Introduction to FSMs: Mealy and Moore machines.
Week 2	Synchronous design process: state diagram, state table with limited number of inputs and outputs.
Week 3	Design examples of FSMs.
Week 4	Synchronous design process: reduction state table and binary assignment table with limited number of inputs and outputs. Design examples of FSMs.
Week 5	Synchronous design process: circuit realization with different types of flip flops.
Week 6	Analysis of synchronous sequential circuits.
Week 7	Student presentations of <u>synchronous</u> circuit design projects.

Week 8	Midterm Exam
Week 9	Introduction to Asynchronous sequential circuits with design methodology: state diagram, state table, reduction, merging table, binary assignment table and circuit realization.
Week 10	Asynchronous vs. synchronous sequential circuits: hazards and races in asynchronous circuits.
Week 11	Asynchronous design process: state diagram, primitive flow table with limited number of inputs and outputs. Design examples of FSMs.
Week 12	Asynchronous design process: reduction, merging table and binary assignment table with limited number of inputs and outputs. Design examples of FSMs.
Week 13	Analysis of Asynchronous sequential circuits
Week 14	Student presentations of <u>Asynchronous</u> circuit design projects.
Week 15	Review of key concepts and preparation for final exam
Week 16	Final Exam

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Introduce basic VHDL concepts and its simulator
Week 2	VHDL description of logic circuits, VHDL models, operators and libraries.
Week 3	Implement different logic gates (AND, OR, NOT) using VHDL dataflow method
Week 4	Implement different logic gates (AND, OR, NOT) using VHDL structure method
Week 5	Implement simple combinational circuit using VHDL, adders and subtractors
Week 6, 7	Modeling other combinational logic components using VHDL structure method, such as Mux, Dmux, Decoder, Encoder, comparator etc.
Week 8	Sequential Circuits - Latches and Flip-Flops using Behavioral modeling
Weeks 9, 10	Implementing SR, D flip-flops
Weeks 11, 12	Implementing JK, and T flip-flops
Weeks 13, 14	Implementing registers and counters using VHDL processes
Weeks 15	Mini Project and/or preparation for involving VHDL in final exam

Learning and Teaching Resources		
مصادر التعلم والتدريس		
	Text	Available in the Library?
Required Texts	- Fundamentals of Logic Design, Charles H. Roth & Larry L. Kinney, all edition until 6th edition in 2010-2014. - William Stalling, "Computer Organization and Architecture" 6th edition.	Y (one version)
Recommended Texts	Digital Design, M. Morris Mano & Micheal D. Ciletti, 4th edition.	N (available online)
Websites	Any VHDL book with digital or logic design on online can be useful.	

APPENDIX:

GRADING SCHEME				
مخطط الدرجات				
Group	Grade	التقدير	Marks (%)	Definition
Success Group (50 - 100)	A – Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C – Good	جيد	70 - 79	Sound work with notable errors
	D – Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E – Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	FX – Fail	مقبول بقرار	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required
Note:				
Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.				