	Ministry of Higher Education and Scientific Research - Iraq AL-Naji University College of Engineering Department of Computer Engineering	

MODULE DESCRIPTOR FORM

نموذج وصف المادة الدراسية

Module Information
معلومات المادة الدراسية

Module Title	**COMPUTER ARCHITECTURE 1**	**Module Delivery**	
Module Type	**CORE**	**Class Lecture + Lab**	
Module Code	**COE 208**		
ECTS Credits	**6**		
SWL (hr/sem)	**150**		
Module Level	2	**Semester of Delivery**	4
Administering Department	Computer Engineering	**College**	Engineering
Module Leader	Mohammed Talal Saleem	**e-mail**	mohammed.talal@alnaji-uni.edu.iq
Module Leader's Acad. Title	Lect. Dr.	**Module Leader's Qualification**	
Module Tutor		**e-mail**	
Peer Reviewer Name		**e-mail**	
Review Committee Approval		**Version Number**	

Relation With Other Modules
العلاقة مع المواد الدراسية الأخرى

Prerequisite module	COE107	**Semester**	2
Co-requisites module		**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	Understand basic computer architecture and hardware. And Explore CPU design and execution methods.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	• Describe key principles of computer architecture, including the function of core hardware components and their interactions. • Recognize and explain the roles of various CPU components, such as ALUs, registers, and caches. • Solve practical problems by applying theoretical knowledge of computer architecture.
Indicative Contents المحتويات الإرشادية	
Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	- Lectures. - Homework and Assignments. - Tests and Exams. - In-class questions and Discussions. - Extracurricular Activities. - Individual / Group Projects - In- and Out-Class conversations.

Student Workload (SWL) الحمل الدراسي للطالب			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	79	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	5
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	71	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	5
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation
تقييم المادة الدراسية

		Time/ Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	**Quizzes**		12% (12)		
	Attendance and Participation		8% (8)		
	Home works		5% (5)		
	Lab.		15% (15)		
Summative assessment	**Mid Exam**	1	10% (10)		
	Final Exam	3 hrs.	50% (50)		
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)
المنهاج الاسبوعي النظري

	Material Covered
Week 1	Register Transfer Language
Week 2	Arithmetic Micro operations
Week 3	Instruction Codes
Week 4	Timing and Control
Week 5	Memory-Reference Instructions
Week 6	Complete Computer Description
Week 7	Design of Accumulator Logic
Week 8	Control Memory
Week 9	Micro program Example
Week 10	Design of Control Unit

Week 11	Central Processing Unit
Week 12	Instruction Formats
Week 13	Addressing Modes
Week 14	Program Control
Week 15	Reduced Instruction Set Computer
Week 16	**Final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	HDL simulator
Week 2	Full Adder
Week 3	Arithmetic circuit
Week 4	Arithmetic, Logic and Shift unit
Week 5	Bus System
Week 6	Registers
Week 7	Memory (ROM)
Week 8	Memory (RAM)
Weeks 9, 10, 11	Hardwired control unit
Weeks 12, 13, 14	Microprogrammed control unit
Week 15	Exam

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	• M. Morris. Mano, "Computer System Architecture" 3rd Edition • William Stalling, "Computer Organization and Architecture" 6th edition.	
Recommended Texts	• P. Trivedi and R. P. Tripathi, "Design & analysis of 16 bit RISC processor using low power pipelining," International Conference on Computing, Communication & Automation, Noida, 2015, pp. 1294-1297. • B. W. Bomar, "Implementation of microprogrammed control in FPGAs," in IEEE Transactions on Industrial Electronics, vol. 49, no. 2, pp. 415-422, Apr 2002. • J. L. Cruz, A. Gonzalez, M. Valero and N. P. Topham, "Multiple-banked register file architectures," Proceedings of 27th International Symposium on Computer Architecture (IEEE Cat. No.RS00201), Vancouver, BC, Canada, 2000, pp. 316-325. • C. Hamacher, Z. Vranesic, S. Zaky, N. Manjikian "Computer Organization and Embedded Systems", Sixth Edition • Computer Architecture A Quantitative Approach, Sixth Edition, John L. Hennessy, David A. Patterson, 2019.	
Websites		

APPENDIX:

GRADING SCHEME مخطط الدرجات				
Group	**Grade**	التقدير	**Marks (%)**	**Definition**
Success Group (50 - 100)	**A** – Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C – Good	جيد	70 - 79	Sound work with notable errors
	D – Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E – Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	مقبول بقرار	(45-49)	More work is required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required
Note:				

NB Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.