	Ministry of Higher Education and Scientific Research - Iraq **Al-Naji University** **College of Engineering** **Department of Cybersecurity Engineering**	

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	Digital Logic Design			**Module Delivery**	
Module Type	S			☒ **Theory** ☐ **Lecture** ☒ **Lab** ☐ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	CSE1107				
ECTS Credits	5				
SWL (hr/sem)	125				
Module Level		UG I	**Semester of Delivery**		1
Administering Department		CSE	**College**	College of Engineering	
Module Leader	Maher Faik Esmaile		**e-mail**	maherfaik3@alnaji-uni.edu.iq	
Module Leader's Acad. Title		Lecturer	**Module Leader's Qualification**		Ph.D.
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name		Mohammed Falih	**e-mail**	m.falih@nahrainuniv.edu.iq	
Scientific Committee Approval Date		11/06/2023	**Version Number**		1.0

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	1. To provide students with essential theory material in digital logic design and practical experience required in digital logic applications. 2. To understand digital logic design fundamentals. 3. This course deals with the basic concept of binary, decimal, hexadecimal, octal numbers, and the conversion between them. 4. To understand the design of combinational logic circuit and digital device. 5. Understand the memory circuits (RAM, ROM PROM, EPROM and EEPROM). 6. Understand the process of programmable of logic circuit. 7. Solve problem related to digital logic design.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	On successful completion of the course the students should be able to: 1. Recognize digital logic design system. 2. Summarize what is meant by a basic digital logic design. 3. Discuss digital logic design fundamentals. 4. Describe binary, decimal, hexadecimal, octal numbers, and the conversion between them. 5. Design of combinational logic circuit and digital device. 6. Discuss algebraic manipulation and analysis of logic circuit using truth tables. 7. Identify the Encoder, Decoder, Multiplexer, and Demultiplexer. 8. Discuss the operations of memory circuits (RAM, ROM PROM, EPROM and EEPROM). 9. Discuss the the process of programmable of logic circuit.
Indicative Contents المحتويات الإرشادية	Indicative content includes the following. **Part A – Digital logic design and Binary System** Digital systems: Decimal, binary, octal, hexadecimal number, number conversions, BCD, binary and hex arithmetic, complements, signed numbers. [8 hrs] **Part B - Boolean algebra and Logic Gates** Boolean algebra and logic gate, Postulates and theorems of Boolean algebra, Operator Precedence, Boolean function, Complement of a Function Gate-level minimization

	combinational Logic, Canonical and standard forms, Minterms, Maxterms, other logic operations. [16 hrs] Algebraic manipulation (Simplification), analysis of logic circuit using truth tables, Simplification of Boolean functions, the map method, two, three, four, five and six variable maps. Product of sum simplification. [12 hrs] **Revision problem classes [2 hrs]** NAND implementation, NOR implementation, don't care conditions. Design of combinational logic circuit, adder, half-adder, full-addedr. Subtractor, half-subtractor, full-subtractor, code conversion. Universal gates NAND, Universal gates NOR. Magnitude Comparator, Decoder. Demultiplexer, Encoders, Multiplexers. [24 hrs] **Part C- memory and programmable Logic [4 hrs]** Random Access Memory (RAM), Read-Only Memory (ROM), Memory Decoding, Programmable Array logic (PAL), Programmable Logic Array (PLA), introduction to sequential circuit.

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering types of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	77	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	5
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	48	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	3
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**125**		

Module Evaluation
تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	2	10% (10)	3 and 10	1,2,3,6,7
	Assignments	1	10% (10)	2 and 12	2,3,4,6
	Projects / Lab.	1	10% (10)	Continuous	All
	Report	1	10% (10)	13	6,7,8
Summative assessment	Midterm Exam	2hr	10% (10)	7	1-6
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)
المنهاج الاسبوعي النظري

	Material Covered
Week 1	Number systems: Decimal, binary, octal, hexadecimal number, number conversions,
Week 2	BCD, binary and hex arithmetic, complements, signed numbers
Week 3	Boolean algebra and logic gate, Postulates and theorems of Boolean algebra
Week 4	Operator Precedence, Boolean function, Complement of a Function
Week 5	Canonical and standard forms, Minterms, Maxterms, and other logic operations
Week 6	Algebraic manipulation (Simplification), analysis of logic circuit using truth tables
Week 7	Simplification of Boolean functions, the map method, two, three, four, five, and six variable maps.
Week 8	Product of sum simplification
Week 9	NAND implementation, NOR implementation, don't care conditions.
Week 10	Design of combinational logic circuit, adder, half-adder, full-adder
Week 11	Subtractor, half-subtractor, full-subtractor, code conversion
Week 12	Universal gates NAND, Universal gates NOR
Week 13	Magnitude Comparator, Decoder
Week 14	Demultiplexer, Encoders, Multiplexers
Week 15	Read-Only Memory (ROM), introduction to sequential circuit

Delivery Plan (Weekly Lab. Syllabus)
المنهاج الاسبوعي للمختبر

	Material Covered

Week 1	Lab 1: Introduction to experiments
Week 2	Lab 2: Logic Gates (NOT, AND, OR, and NAND)
Week 3	Lab 3: Logic Gates (NOR, XOR, and XNOR)
Week 4	Lab 4: Combinational Logic Circuits: Simplification of Boolean Functions
Week 5	Lab 5: Karnaugh Maps, Don't Care
Week 6	Lab 6: Code Conversion
Week 7	Lab 7: Basic Arithmetic Operations: Half-Adders, Half-Subtractor
Week 8	Lab 8: Basic Arithmetic Operations: Full-Adders, Full-Subtractor
Week 9	Lab 9: Magnitude Comparator
Week 10	Lab 10: Design of Digital Devices (Decoder)
Week 11	Lab 11: Design of Digital Devices (Encoder)
Week 12	Lab 12: BCD to Seven Segment
Week 13	Lab 13: Multiplexer
Week 14	Lab 14: Demultiplexer

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Digital Logic and Computer Design, M. Morris Mano, Pearson Education © 2017.	
Required Texts	Digital Fundamentals, Thomas L. Floyd, Prentice-Hall, 11th Edition, 2015.	
Recommended Texts	Digital Design, M. Morris Mano, 5th Edition, 2013	
Websites		

Grading Scheme
مخطط الدرجات

Group	Grade	التقدير	Marks %	Definition
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.